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State of Charge Equalization of Battery Modules Using Single-Phase Cascaded Multilevel Converters

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Abstract— This paper aims to use cascaded multilevel converters for connecting several battery modules to a single-phase AC grid or load. Electrical power is exchanged either from storage to AC side to discharge battery modules, or from AC side to the storage to charge battery modules. Charging and discharging operations are performed while battery modules' state of charges get equalized. AC side current is also controlled to follow its reference while high differential-mode dv/dt on load are avoided using adjacent voltage levels assignment. For these purposes, no additional controlling circuit is implemented and only one controlling block is defined to handle AC current reference tracking, and state of charge balancing tasks. Model predictive control, as a technique capable of multi-parameter controlling, is used to achieve beforementioned system objectives in a simple, efficient, and scalable manner. MATLAB Simulink simulations demonstrate the feasibility of proposed controlling strategy for this sort of application.

Keywords— cascaded multilevel converters, battery balancing, state of charge, model predictive control

I. INTRODUCTION

Towards achieving the goal of CO₂ emissions reduction [1], and to fulfill new consumer demands, a large variety of battery storage applications are introduced while the penetration of Li-ion batteries in today's electric energy market [2] for power systems and electric vehicles is inevitable [3] [4]. For most of the applications, a combination of multiple battery cells are connected in series or parallel to each other forming a high energy or power storage cluster i.e. battery pack [5]. Another alternative for pack formation is to connect multiple cells into modules, and connect multiple modules to form a pack [6].

Battery management systems (BMS) are implemented on battery packs to maintain the storage cluster in an accurate and reliable operational condition by performing several tasks such as voltage, current, and temperature measurement, state of charge (SoC), health (SoH), and remaining useful life (RUL) estimation, cell protection, thermal management, charge/discharge control, data acquisition, communications, and cell or module balancing [7]. The latter is considered to be a crucial task for BMS as after many charge and discharge cycles, imbalance cell SoCs lead to major failures caused by overcharging and deep discharging of individual cells or modules [8]. These failures cause deterioration in system performance and energy loose in the storage cluster. Cells/modules with lowest SoC reach the lower safe voltage limit in prior to others which force the BMS to stop discharging operation. In contrary, cells/modules with highest SoC reach the upper safe voltage limit in prior to others which force the BMS to stop charging operation [9]. Imbalance SoCs

between similar cells or modules within a battery pack is caused by production-related differences and different operational and environmental conditions [10].

Cell balancing topologies are mainly categorized as passive and active approaches [11]. While passive method dissipates redundant energy of cells with higher SoCs, active method transfers the redundant energy from cells with higher SoC to cells with lower SoC to equalize all cells or modules within a battery pack. A recent approach is to take advantage of multilevel converters to directly connect storage cluster to AC side e.g. grid or load. This method avoids a common DC link and integrates independent battery modules into each cascaded H-bridge cell [12]. Depending on application, this method benefits from lower power rate of switches, lower LC filter stored energy, high reliability and fault tolerance owing to its modular structure [13]. Although the best characteristic of this approach is that does not require any additional circuitry or dedicated control diagram to perform battery balancing operation.

This paper introduces a scalable controlling approach for multiple battery modules to be directly connected to single-phase AC side using a multilevel cascaded H-bridge converter. The single control diagram is designed to achieve multiple objectives of maintaining AC side parameters i.e. current reference following, battery SoC equalization, and prevention of high differential-mode dv/dt during transients to avoid damage in particular applications such as electric drives [14]. Model predictive control (MPC) is used in the control diagram to fulfill the mentioned tasks in a simplified manner while it is modified to have a significant decrease in computational load. This technique is preferred over other control techniques for the current work as MPC benefits from multivariable control capabilities, fast dynamic response, ease of implementation and flexibility [15] while converter switches are directly manipulated without the presence of a modulator [16]. The latter feature is particularly exploited in this study to integrate SoC balancing capability into the diagram.

The rest of the paper is organized as follows. The cascaded H-bridge converter with integrated energy storage configuration is introduced and modelled in Section II. Based on the modelling, the control strategy alongside SoC balancing capability is thoroughly described in Section III. Finally, Section IV demonstrates simulation results under different scenarios to investigate the feasibility of the proposed approach, leading to Section V which concludes the study.

II. SYSTEM MODEL AND CONFIGURATION

The proposed controlling method requires precise modelling of system components including the converter and grid/load. Battery modules' modelling and state of charge estimation are out of the scopes of this paper. Fig. 1 demonstrates the system configuration for n number of cells in a single-phase storage cluster. Each cell is composed of a battery module and four switches as depicted in the figure. Output voltage of each cell is v_n while the converter's output voltage v_o is formed by series connection of cells. The storage cluster is connected to single-phase grid/load through an RL filter. Considering that the proposed method is extendable to n number of cells in a storage cluster, the case study defined for this paper includes five cells in the storage cluster.

Each switch $S = \{S1_n, S2_n, \bar{S}1_n, \bar{S}2_n\}$ either takes a binary value of 1 or 0 indicating *ON* or *OFF* states respectively. Individual cells are able to generate output voltage of $+V_{batt}$ while $S1_n = 1$ and $S2_n = 0$, $-V_{batt}$ while $S1_n = 0$ and $S2_n = 1$, and 0 while $S1_n = S2_n$. Consequently, output voltage of the converter is obtained from the equation below:

$$v_o = \sum_{x=1}^n v_x = \sum_{x=1}^n V_{batt}(S1_x - S2_x) \quad (1)$$

Having n cells in each cluster, $(2n + 1)$ voltage levels are produced in a staircase shaped waveform for a single-phase sinusoidal reference with level variations demonstrated in Fig. 2. In the current case study, eleven levels of $\{-5V_{batt}, -4V_{batt}, \dots, 0, \dots, +4V_{batt}, +5V_{batt}\}$ are generated. Corresponding to possible output voltages mentioned, a set of control indexes i.e. switching orders U are defined as:

$$U_{(2n+1)} = [u_1, u_2, \dots, u_{2n+1}]^T \quad (2)$$

where $u \in \mathbb{Z}$ varies in the range of $[-n, +n]$ which in this paper the range is $[-5, +5]$ as there are five cells in the storage cluster. While the set of S indicates the individual cells' switches states with binary values, each element of U indicates a control index for the whole storage cluster. For instance, index of $u = -4$ defines that four out of five battery modules are connected in reverse poles and one is bypassed, $u = 5$ defines that all battery modules are connected in their

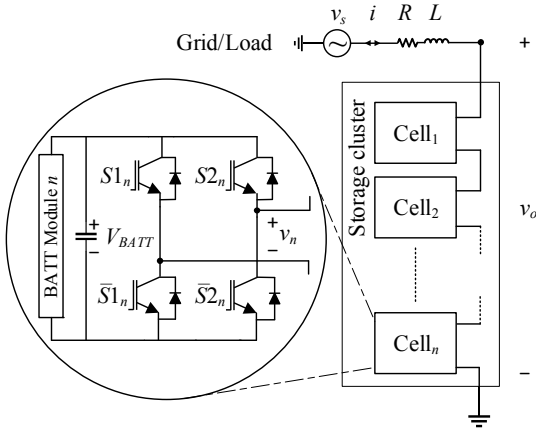


Fig. 1. System configuration

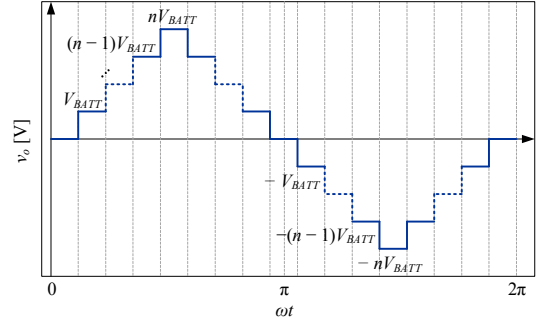


Fig. 2. Generated output voltage levels of the cascaded converter following a sinusoidal current reference.

nominal poles, and $u = 0$ defines that all battery modules are bypassed. Referring to Fig. 1, converter output voltage v_o is derived through the first order current equation as:

$$v_o = Ri + L \frac{di}{dt} + v_s \quad (3)$$

The equation above will be used as a base to the controller design in next sections together with (1). It should be noted that batteries' output voltages V_{batt} are assumed constant while charging and discharging since the proposed control method has minor dependency to V_{batt} variations in different SoCs.

III. CONTROL APPROACH

The primary control objective is to have exchanged current i following its defined reference, while battery modules' SoCs get equalized. Meaning that the controller must be able to share the extracted/injected power between battery modules during discharging or charging operations respectively and maintain AC side's current. Power sharing is done respecting battery modules SoC through direct manipulation of cell switches set S . An additional objective is defined for the controller to avoid large voltage variations during transients and also reduce computational load on the processor by assigning adjacent voltage levels. Since the control problem of this study has become multi-objective, model predictive control (MPC) is selected to overcome any possible challenges.

A. Predictive Controller

MPC considers the model of the system, and corresponding to the model, predicts every possible behavior of the system output. The one control index that leads to minimum deviation between desired output and predictions, is chosen to be applied for next instant. This process is done in a discrete timeframe. Consequently, the system model has to be discretized using the Euler forward estimation as:

$$y_{k+1} \approx y_k + T_s f(y_k, t_k) \quad (4)$$

in which t_k is time at k th step, y_k is the computed solution at t_k , T_s is the timestep size or duration between two consecutive sampling intervals defined as:

$$T_s = t_k - t_{k-1} \quad (5)$$

Using (4), discretization of (3) becomes as:

$$i[k+1] = i[k] \left(1 - \frac{T_s R}{L}\right) + \frac{T_s}{L} (v_o[k] - v_s[k]) \quad (6)$$

this equation demonstrates that future behavior of i is a function of current value of it, with addition of a second term consisting current values of converter output voltage. The latter term is derived from the eleven control indexes u_1 to u_{11} in set of U introduced in previous section. Therefore, in each sampling period, eleven predictions are calculated and the one control index which generates the least deviation to the reference i^* , is selected to be applied in the beginning of next sampling interval. Evaluation of predicted values are done using the cost function J as below:

$$J[k+1] = |i^*[k+1] - i[k+1]| \quad (7)$$

where the estimation of $i^*[k+1] \approx i^*[k]$ can be used to achieve $i^*[k+1]$ since the sampling period T_s is too small. Finally, best control index u^* to be applied in next interval is defined as:

$$u^*[k+1] = \operatorname{argmin} J[k+1] \quad (8).$$

So far, the controller is able to follow reference signal in each sampling interval. While a loop of $(2n+1)$ predictions and cost function evaluations are executed in every T_s , the number of loop iterations might get large for higher amounts of cells in the storage cluster. This will significantly increase the computational load for the controller. To overcome this challenge, predictive controller can be modified in a way that instead of all possible voltage levels, only adjacent voltage levels get processed in each interval as by observing the steady state behavior of the converter output in Fig. 2, it can be concluded that for a sinusoidal reference, output voltage is shaped like a staircase that in each consecutive timestep, adjacent voltages are applied. Adjacent levels and their corresponding control indexes are assigned as:

$$\sqrt{(v_o)^2 + (v_{adj})^2} \leq V_{BATT} \quad (9)$$

denoting that for every voltage level, all other levels having maximum distance of V_{BATT} to it, will be assigned as an adjacent level to that voltage level. Therefore, number of computations in each sampling interval will decrease from $(2n+1)$ to 3 (i.e. current voltage itself, plus the level before and the level after). It should be noted that for highest and lowest levels of voltages, there will be only two adjacent levels assigned since there are no more levels above or below them, respectively. Depending on application, adjacent levels' selection diameter can be manipulated to assign more adjacent voltages to each voltage level e.g. itself, plus two levels above and two levels below.

Adjacent level assignment also brings the advantage of lower dv/dt during transients since it slows down the output transition from one voltage level to another level more away than V_{BATT} .

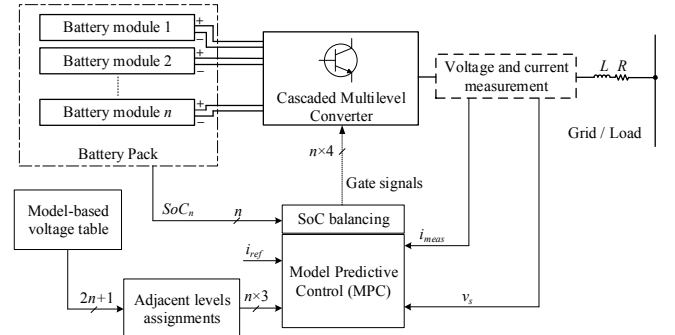


Fig. 3. Overall proposed control diagram.

In Fig. 3, the controlling approach is summarized as a diagram. AC side current i_{meas} and voltage v_s , along with an array of SoCs are measured and imported. Voltage levels table and their corresponding indexes are calculated offline and stored in memory for MPC to access. Reference current is a sinusoidal value with user-defined magnitude and frequency which is imported to the MPC block as well. Control indexes which are outputs of the MPC, are delivered to an SoC equalization block to perform the battery modules balancing by directly sending an optimal set of binary values S to the switches.

B. Balancing Term

It is an inherent degree of freedom provided by cascaded converters that the controller specifies the number of cells to be connected (either in nominal or reversed poles) in each timestep, but it doesn't specify which cells. This point is exploited in this section to aim for equalization of SoCs. It should be noted that control indexes of $u = (-n)$, $u = 0$, and $u = n$ provide no degree of freedom for balancing in this method since the define all cells to be connected or all cells to be bypassed. Rest of indexes can be applied in a way described below to achieve balanced battery modules.

The SoC equalization block applies optimal control indexes $u^*[k+1]$ after being generated in cost function output to the switches by feeding them a set of binary values S in every timestep T_s . Primarily, a set of battery modules' SoCs are imported as:

$$SoC = \{SoC_1, SoC_2, \dots, SoC_n\} \quad (10)$$

for n number of cells in the storage cluster continuously. Elements of SoC get sorted as a new set of $\mathbb{T} = \operatorname{sort}(SoC)$ and depending on high or low SoC modules, the block decides which cells to be bypassed, or which cell to be connected in either nominal or reversed poles. Binary values to $S1$ and $S2$ switches of n cells are defined as below for discharging operation:

$$S1_n := \{1 | \forall u^*[k+1] \neq \{-n, 0, n\}, \\ SoC_n \in \mathbb{T}^{|u^*[k+1]|} \wedge S2_n = 0\} \quad (11)$$

and for charging operation:

$$S1_n := \{1 | \forall u^*[k+1] \neq \{-n, 0, n\}, \\ SoC_n \in \mathbb{T}_{|u^*[k+1]|} \wedge S2_n = 0\} \quad (12)$$

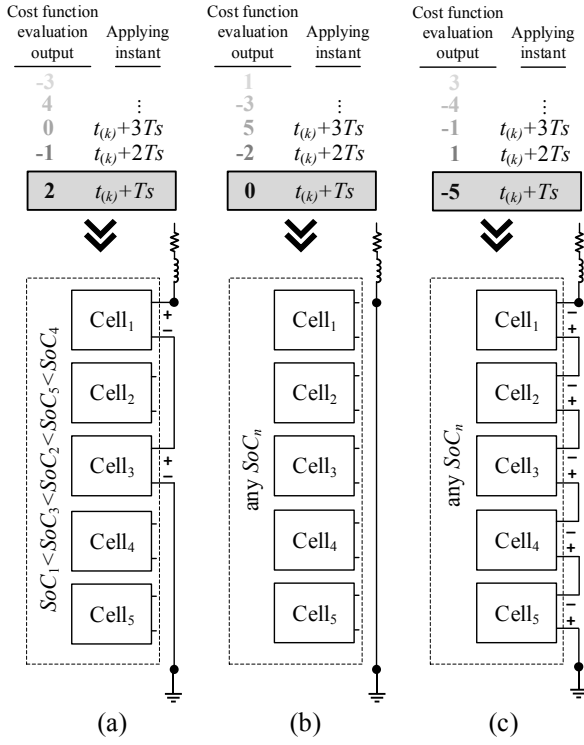


Fig. 4. Applying control indexes from cost function to switches to perform SoC balancing (a) index of 2 (b) index of 0 (c) index of (-5) .

where $\mathbb{T}^{|u^*[k+1]|}$ and $\mathbb{T}_{|u^*[k+1]|}$ denote the last and first $|u^*[k+1]|$ elements of \mathbb{T} , respectively.

Both (11) and (12) are generic equations for a proposed system with n cells per storage cluster. The main idea these equations is that higher SoC battery modules prioritized to be connected during discharging operation, and lower SoC cells prioritized to be connected during charging operation. Fig. 4 demonstrates three examples of connecting/bypassing cells based on (12) for charging operation. In Fig. 4(a), the control index of $u^*[k+1] = 2$ is selected by MPC to be applied in the beginning of next timestep. The first two elements of \mathbb{T} are SoC_1 and SoC_3 , hence $Cell_1$ and $Cell_3$ are connected in nominal poles. In Fig. 4(b), $u^*[k+1] = 0$, hence there is no degree of freedom for balancing since the controller must bypass all the cells. In Fig. 4(c), $u^*[k+1] = (-5)$ thus similar to Fig. 4(b), \mathbb{T} is disregarded and all five cells are connected in reversed poles.

IV. RESULTS AND DISCUSSION

Five Nickel Manganese Cobalt (NMC) battery modules are connected to grid/load using a single-phase cascaded converter in MATLAB Simulink platform to demonstrate the feasibility of the proposed approach. System behavior under both charging and discharging operations are observed and investigated. In all simulations, initial SoC of five battery modules are 48%, 54%, 50%, 56%, 52% in $Cell_1$ to $Cell_5$, respectively. Consequently, initial deviation between highest and lowest SoCs is 8% in all scenarios. The rest of simulation parameters are summarized in Table I.

SoC variations within the system while charging and discharging operations are shown in Fig. 5. There is a scenario defined for Fig. 5(a)&(b) where the storage cluster gets charged for first 200s, then changes into discharging mode and

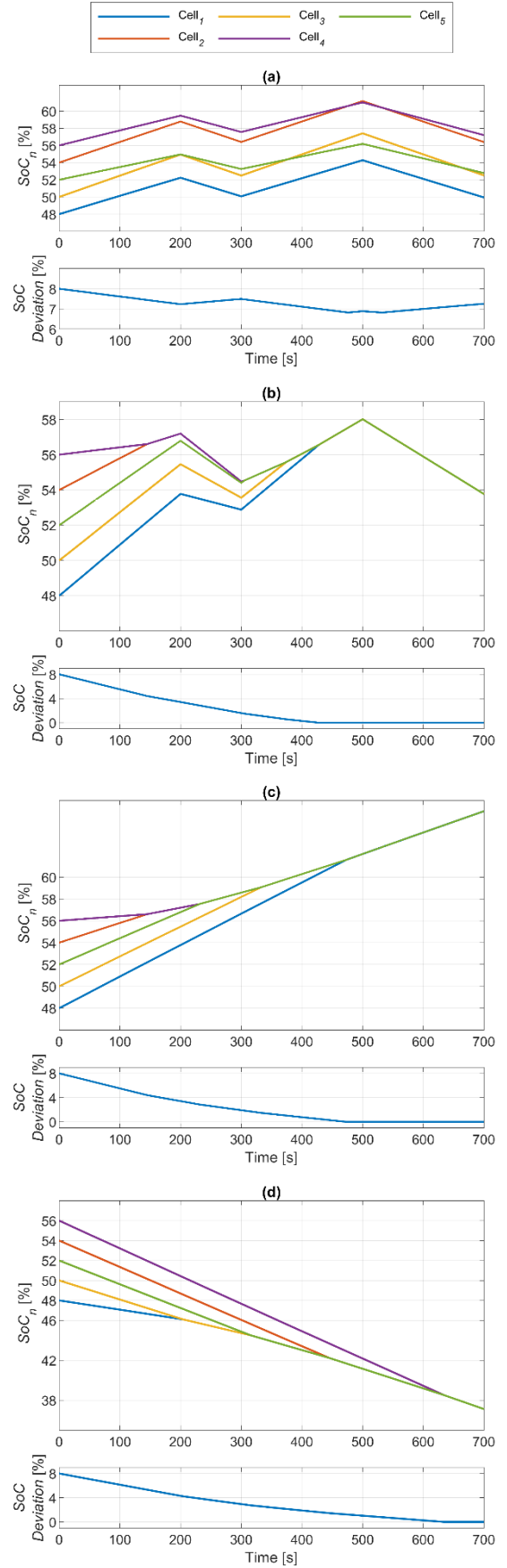


Fig. 5. Battery modules' SoCs and their corresponding deviation between highest and lowest SoCs for four scenarios of (a) no balancing control applied while charging and discharging (b) balanced operation while charging and discharging (c) balanced operation while constantly charging and (d) balanced operation while constantly discharging.

TABLE I. SYSTEM PARAMETERS

| Parameter | Value |
|---|-----------------|
| Battery modules quantity n | 5 |
| Battery modules' capacity | 3 Ah |
| Sampling period T_s | 60 μ s |
| Filter resistance R | 0.1 Ω |
| Filter inductance L | 0.9 mH |
| Battery modules terminal voltage V_{batt} | 19 VDC |
| Grid/Load peak voltage | 60 $\sqrt{2}$ V |
| Reference current magnitude i_{ref} | 5 A |
| Grid/Load fundamental frequency | 50 Hz |

keeps discharging for the next 100s. Again, on $t = 500$ s mode change takes place. This scenario is defined to observe and ability of control approach to switch online between charging and discharging modes. As it can be seen on Fig. 5(a), while there is no balancing block in the control diagram, SoCs change randomly without converging and deviation is even increasing in some periods. Fig. 5(b) demonstrates the system operation for same mode change scenario with balancing block applied into the control diagram. From the starting point, SoCs are converging and deviation percentage is decreasing continuously. While the operation mode is changed to discharging, SoC convergence is not interrupted and module SoCs get converged into each other one by one. Finally, at $t = 420$ s, SoCs are balanced and keep charging and discharging in the same equalized manner. Balancing control is continuously applied and SoCs doesn't diverge as the deviation is kept on 0%. Fig. 5(c)&(d) demonstrate the same desired behavior of the system while constantly charging and discharging respectively.

Corresponding to the operation scenario applied in Fig. 5(a)& (b), averaged currents derived or injected from/to battery modules are depicted on Fig. (6). As in Fig. 6(a), in case there is no SoC balancing, current sharing ratio remains constant either while charging or discharging. But as in Fig. 6(b), the control diagram dynamically changes the currents share of different modules according to SoC values to get all modules balanced. Meaning that higher SoC modules deliver more current while discharging and get less current while charging. Eventually at $t = 420$ s, module currents get equalized and the charge and discharge by the same current ratio as the control objective i.e. SoC balancing is reached.

Fig. 7 shows AC side parameters of converter output voltage and output current behavior. During charging operation, current waveform is in 180° phase difference with

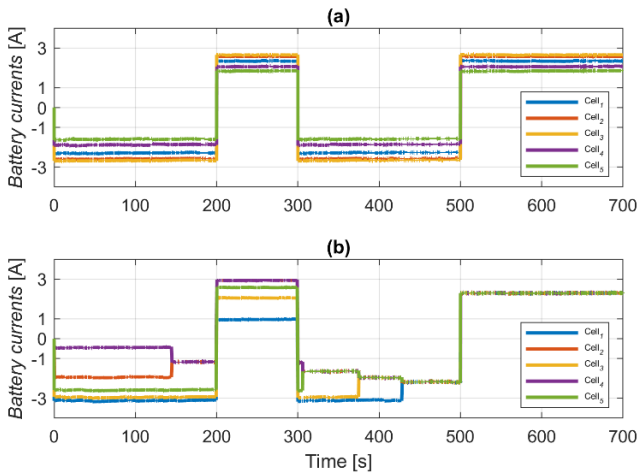


Fig. 6. Averaged currents exchanged by battery modules during charge and discharge operations (a) while no balancing control applied (b) while SoC balancing is applied.

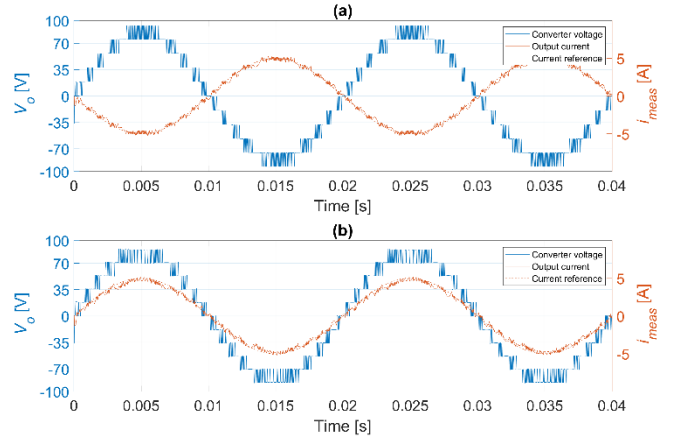


Fig. 7. Converter output voltage alongside AC side current i while (a) charging and (b) discharging operations.

output voltage while in discharging operation, output current and voltage are in equal phase. In either operation, current waveform has followed its reference properly and eleven levels of output voltage is generated by the converter.

The effect of adjacent voltage levels assignment is clearly demonstrated during a transient scenario defined in Fig. 8(a). There is step change in current reference from 5 A to 7 A meanwhile discharging mode is switched to charging mode.

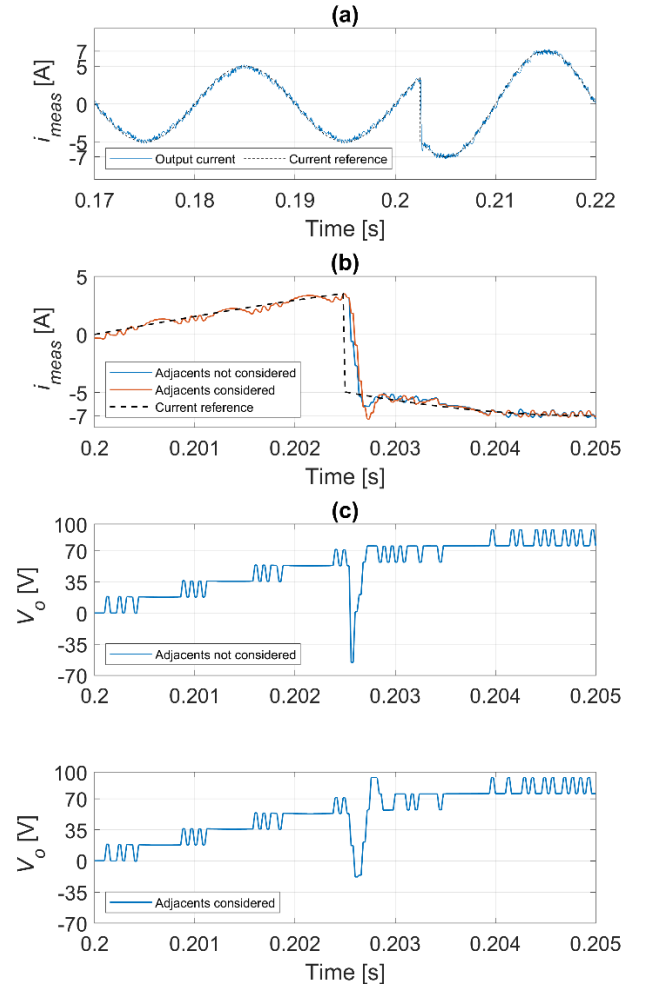


Fig. 8. Output current and voltage behavior of the converter for a transient scenario defined in (a), while (b) denotes a comparison of current response between considered and unconsidered adjacent cases and (c) denotes a comparison between output voltage behaviour between considered and unconsidered adjacent case.

Although it is unlikely to have this scenario in real applications, but this section aims to demonstrate the benefits of adjacent voltage level assignment in a severe transient. Fig. 8(b) shows the behavior of output current during the step change. Controller has been able to follow reference current and its response is fast. While the output voltage shows a big and sudden change from $+57\text{ V}$ to -57 V in Fig. 8(c) during one T_s , indicating a huge dv/dt which is not the desired case for some applications. The behavior of beforementioned parameters in Fig. 8(c) demonstrates that in case of adjacent levels assignment, total output voltage change is from $+57\text{ V}$ to -19 V . Not only the magnitude of the change is much less than unconsidered adjacent case, but this change has occurred within three periods of T_s , which denotes much less and slower dv/dt variation. Output current has also followed its reference during the transient with a slightly lower speed comparing to unconsidered adjacent case which is negligible. Slower current response is justifiable since the controller does not allow sudden change in voltage.

V. CONCLUSION

A single-phase storage cluster is implemented using bidirectional cascaded converter which directly connects battery modules to the AC side either it could be grid or load. Battery modules are charging and discharging while output parameters are maintained and following their references. Meanwhile the control diagram performs the charge or discharge operations while battery modules' SoCs get equalized. Also, converter output voltage follows a strategy that avoids big changes with smaller dv/dt and decreases computational load of the controller. These three control objectives are achieved by using model predictive control technique which benefits from multi-parameter controlling capability. Main advance of the proposed approach is that no additional circuitry and control diagram is needed to achieve SoC balancing and converter control diagram by itself can reach storage side, and AC side objectives in a feasible way as demonstrated in results section. Sensitivity analysis of the control term to parameters' variations e.g. battery voltages, inductance and resistance, alongside comparison between similar approaches using different control techniques can be further steps for future work.

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